micross
one source. one solution.®

Adv. Interconnect Technology

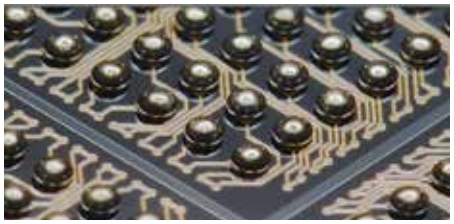
Service Overview

Micross Advanced Interconnect Tecnhology (AIT) provides development, custom prototyping and production services, as well as unique solutions to challenge interconnect and packaging requirements for a wide variety of commercial, private, government, and hi-rel customers.

INTEGRATION & ADVANCED PACKAGING SOLUTIONS

Micross AIT has been at the forefront of the development of such interconnect and packaging technologies for more than 25 years, making them accessible to external organizations for a wide variety of advanced and low-volume applications. We provide application based solutions for government and industry clients in technology areas such as high-performance sensor and actuator arrays, biomedical devices and high-performance computing. Some of our integration & packaging technologies include:

- 3D Integration Technology: Through Silcion and Through Glass Vias, Si Interposers and 3D IC
- Advanced Interconnect and Packaging Technologies: Solder Bumping, Cu Pillar, Cu-Based Microbumps and Assembly
- Microstructure Fabrication and Packaging: Monolithic Integration, Novel Microfabrication and Wafer-Level Vacuum Packaging



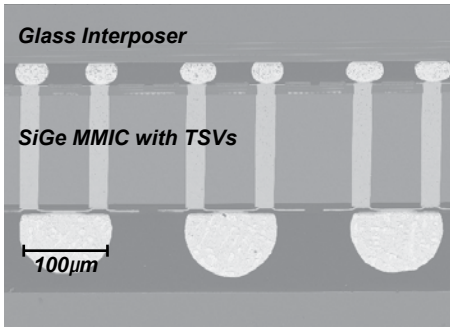
2.5/3D HETEROGENEOUS INTEGRATION

Micross AIT is a leader in heterogeneous integration technology, having developed a broad range of 2.5D and 3D process capabilities and achieved successful demonstrations of 3D-integrated IC stacks for IR focal plane arrays and silicon interposers for embedded computing modules. We've been developing and implementing heterogeneous integration technologies since 1999, building on decades of experience in the development of advanced microfabrication and packaging technologies.

Micross AIT collaborates with a wide variety of clients and partners, bringing integrated process, design, testing and analysis capabilities to projects involving custom application-driven development and access to our 2.5D/3D technology platform through joint development projects, prototyping services and small volume production.

Micross AIT 2.5D/3D integration technology platform is based on several enabling process modules, which include;

- Through-Silicon Via (TSV) Interconnects:
- High Density 3D IC Applications, Filled 2-20µm Diameter, Up to 10:1 Aspect Ratio
- Wafer Thinning (to < 20µm Si Thickness) & Processing on Temporary Carrier Wafer
- Flip-Chip and High-Density Metal-Metal Interconnects and Assembly, Down to <10µm Pitch
- TSV-Last Processes for TSV Insertion into CMOS Device Wafers and Wafers with High Density BEOL Metal Routing Layers



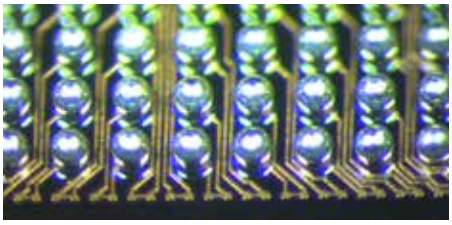
One Source for Innovative Next-Generation Packaging Solutions

WAFER LEVEL PACKAGING

Micross AIT is a leading US-based premier wafer bumping and wafer level packaging facility with 25+ years of experience in developing and providing next-gen interconnect and integration technologies to customers around the world.

Solder Bumping & Wafer Level Chip Scale Packaging

- WLCSP Ball Place, Electroplated C4 and Cu Pillar Bumping with Bump Diameters as Small as 25 micron
- Single and Multiple Layer Cu Redistribution with Several Polymer Repassivation Material Choices
- Eutectic Sn/Pb, Pb-Free and High-Pb Solder Alloys
- Design Services and Custom Test Vehicle Fabrication



Wafer Bumping

Electronic Material Characterization & Process Development

Micross AIT's extensive experience in flip chip and wafer level packaging makes us an ideal partner for suppliers developing new materials for advanced packaging, such as photo-resists, polymer dielectrics, plating chemistries and under-fills.

- Process Characterization and Optimization
- Implementation Into Process Flows
- Test Vehicle Fabrication and Reliability Testing

Flip Chip and Multi-Chip Module Assembly

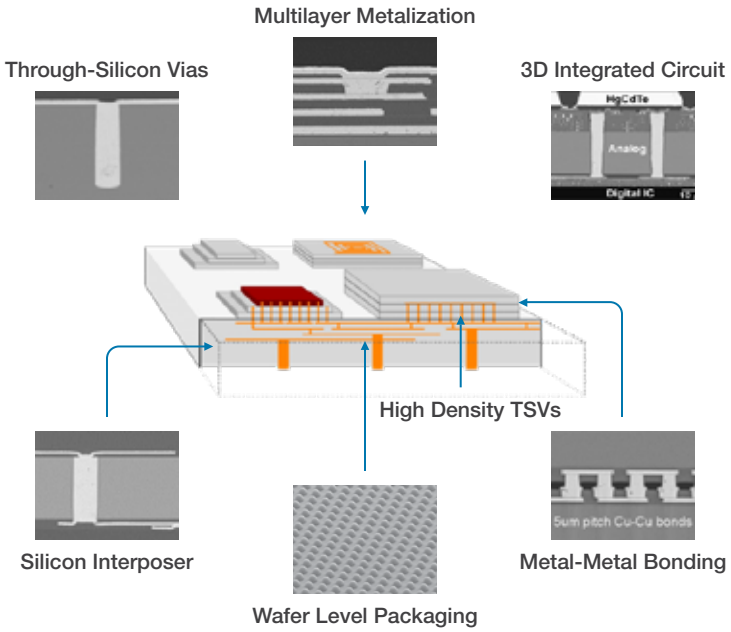
From single chip placements to multi-chip module and system-in-package assembly of multiple die and components, we offer a wide array of capabilities:

- Flip Chip Assembly for Single & Multi-Chip Applications
- Precision Die Placement with Accuracies Better Than +/- 0.5 micron
- Heterogeneous Integration with Si, III-V, and Other Device Types
- Plasma Assisted Dry Soldering (PADS) Process Enables True Fluxless for Assembly for Sn-Bearing Solders

Metal-Metal Bonding for 2.5/3D Technologies

- 2.5D and 3D Integration Technologies are Driving the Integration of Devices with Extremely High Interconnect Densities for Si Interposer and Chip Stacking Applications
- Solid/Liquid Inter-Diffusion Assembly with CuSn-Cu Bump Arrays Demonstrated Down to 10 Micron Pitch
- Cu/Cu Thermo-Compression Bump Bonding Demonstrated Down to 5 Micron Pitch
- Solutions for Chip Stacking and High Thermal Stability Interconnects that Remain Stable at High Temperatures

Customers can take advantage of the 2.5D/3D integration technology platform to realize more highly integrated micro-systems with increased functionality, short interconnect length and decreased size, weight and power (SWaP). From design and fabrication of custom test vehicles to application of 3D integration processes modules on fully functional IC wafers, Micross AIT can provide a variety of integration solutions to meet specific project needs.



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