First Generation NED (Technograph)

Nuclear Event Detector

Part Number: MP13366/002

Rad-Hard

Data Sheet

Defense Specifications for legacy and new equipment often include a nuclear hardening requirement to ensure survival and correct operation of non-hardened electronics following a nuclear event. The First Generation (Technograph) Nuclear Event Detector (NED) provides an output that asserts in response to gamma radiation. This output can be used to protect electronic components. During gamma radiation, damage to both insulated gate (MOS) and PN junction (bipolar) devices may occur. The effects on electronic components can include, for example, reduction of gain, data corruption and the production of photocurrents which may cause latchup and burnout.

Key Features

- Gamma Dose Rate Sensitivity Threshold Range Adjustable from 1 x 10^6 to 10^7 cGy/s at 25°C
- Dual In-Line Package
- Open Collector Outputs
- Radiation Specifications
  - Total Dose (Device Survivability): 1 x 10^4 cGy/s
  - Dose Rate (Operate Through): 2.5 x 10^9 cGy/s
  - Neutron Fluence (Device Survivability): 10^{12} neutrons/cm^2
- 5V Power Requirement
- -55 to +125°C Temperature Range
- BS9450 General Level or MIL-STD-883C Method 5008 Class B Screening Levels

Benefits

- Cost Effective Solution for Nuclear Event Protection
- User Adjustable Delay or “Lock-Out” Time, Selected by Choice of Single External Capacitor
- Use Output Signal to Shut Down Power Supplies, Take Processors Off-Line and Block Memory Write Operations
- Incorporated Event Latch Offering Interfacing with the System Bus, Initiating Software Recovery, or Alerting the CPU

Applications

- Aircraft and drones
- Missiles and bombs
- Satellites
- Military ground vehicles
- Nuclear material storage

Revision History

Revision	Description	Release Date
1.0	MP13366/001Datasheet	05/28/2025
1.1	Changed part number from MP13366/001 to MP13366/002.	01/07/2026

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1.0 Description

The First Generation (Technograph) NED output can be used to remove power, reset processors, disable memory write operations, or simply flag the system that a nuclear event has occurred. Using a PIN diode coupled to an amplifier, the NED can be programmed to respond to a variety of gamma dose rate levels. An event latch is also incorporated, which can be reset by the CPU after system re-initialization. The output of this tri-state latch offers the system designer a variety of options, including interfacing directly with the system bus, initiating software recovery or alerting the CPU to the possibility of corrupt data.

An open collector output gives the subsystem designer flexibility in methods of achieving the specified level of protection. The NED also has a user adjustable delay or "lock-out" time which is selected by the choice of a single external capacitor. Following this delay, the open collector output reverts to the pre-event state, thus enabling the system to be re-initialized allowing successful mission completion.

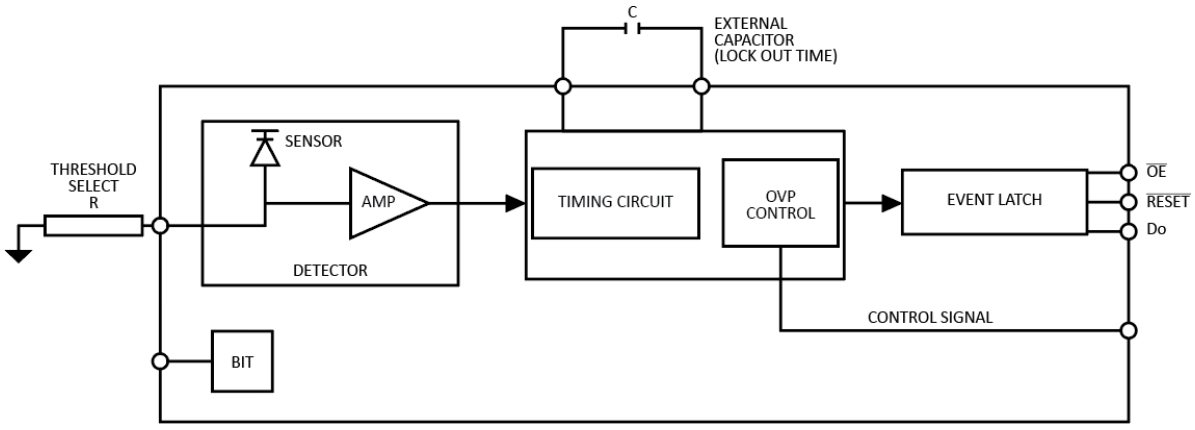

Figure 1. Nuclear Event Detector (NED) Functional Block Diagram

2.0 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings	
Parameter	**Value**
PIN Diode Bias Voltage	+40V max
Open Collector Output Pullup Voltage	+40V max
Nuclear Specifications (survivability)	
Gamma Dose Rate	> 2.5 x 10^9 cGy/s
Gamma Total Dose	1 x 10^4 cGy
Neutron Fluence	> 10^{12} n/cm^2
Operating Temperature	-55 °C to + l25° C
Storage Temperature	-66 °C to + 150° C
Resistance to Solder Heat	350 °C (3 seconds)

3.0 Electrical Specifications

Table 2. Electrical Specifications	
Parameter	**Value**
Operating Voltage	+5V ±0.5V
Quiescent Current	45 mA Typical 72 mA max
Operating Current	65 mA Typical 95 mA max
Open Collector Output Current Sink Capability Voltage Rating	 4mA at 2 x Threshold (Active Low) 40V max
Lockout Time	User Adjustable from 10 µs to 10 ms
Propagation Delay	< 60ns at 10x Threshold
BIT Activation	0V at 100mA sink for > 50 µs
PIN Diode Bias Voltage	+5V Typical +40V max
Dose Rate Threshold Adjustment Range (PIN diode bias voltage = +5V)	10^6 to 10^7 cGy/s at 25° C

4.0 Pinout and Signal Description

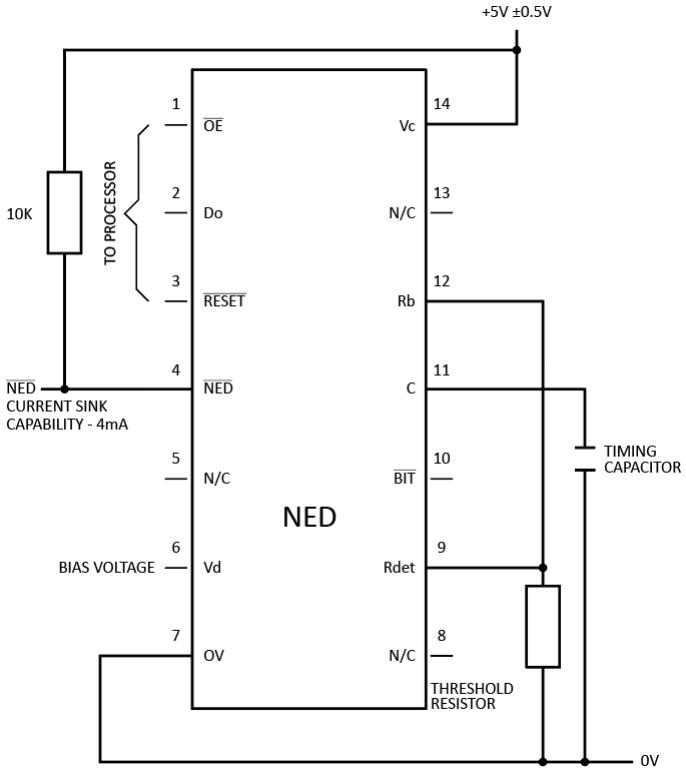

Figure 2. Pinout Diagram

Table 3. Signal Pinout and Descriptions		
PIN Number	**Signal Name**	**Description**
1	$\bar{\bar{O}}\bar{\bar{E}}$	Latch output enable
2	Do	Event latch output
3	$\bar{\bar{R}}\bar{\bar{E}}\bar{\bar{S}}\bar{\bar{E}}\bar{\bar{T}}$	Latch reset
4	$\bar{\bar{N}}\bar{\bar{E}}\bar{\bar{D}}$	Open collector output driver
5	N/C	Not connected
6	Vd	Bias voltage to detect (Up to 40V)
7	0V	Common 0V line (GROUND)
8	N/C	Not connected
9	Rdet	Threshold adjustment resistor connection
10	$\bar{\bar{B}}\bar{\bar{I}}\bar{\bar{T}}$	Active low TTL signal > 50µs to initiate
11	C	Lockout timing capacitor connection
12	Rb	Base connector to input stage

Table 3. Signal Pinout and Descriptions		
PIN Number	**Signal Name**	**Description**
13	N/C	Not connected
14	Vc	Detector supply

5.0 Mechanical Specification

All packages are Nitrogen filled, hermetically sealed, Nickel plated Kovar

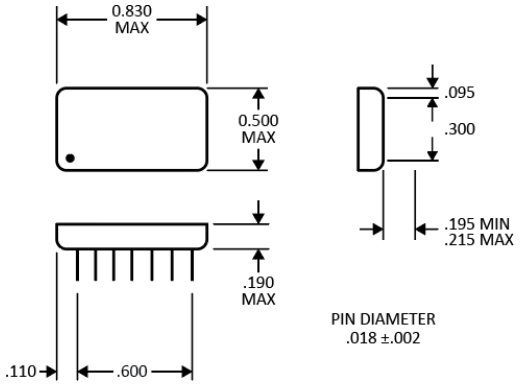

Figure 3. Dual-in-Line Package

6.0 Quality Specification

Each NED Hybrid is 100% screened as detailed below to either BS9450 General Level or MIL-STD-883C Method 5008 Class B.

The NED meets environment qualification testing detailed in BS9450 Full Assessment Level and MIL-STD-883C Method 5008 Class B.

Table 4. Quality Specifications	
Parameter	**Description/Value**
Burn-In	168 hrs. at +125° C
Stabilization Bake	24 hrs. at +150° C
Rapid Change of Temperature	-65 °C to +150° C (10 cycles)
Constant Acceleration (Y axis)	5000 g
Fine Leak	1 x 10^{-7}atm.ccs/sec (He)
Gross Leak	Bubble Test at +125° C
Terminal Robustness	Bending
Endurance / Life Test	2000 hrs at +125° C
Swept Frequency Vibration	100Hz to 2kHz 20g (15 Cycles)

7.0 Reliability

Predicted MTBF is: 1.5 x 10^6 hrs. (Air Inhabited Fighter Environment, Temperature = 80 °C)

8.0 External Component Selection

The radiation threshold sensitivity and lockout time of the NED are user programmable by adjusting the values of external components. Guidance on the selection of suitable component values is given in the following sections.

9.0 Detection Threshold

Figure 4 shows the relationship between the threshold resistor value and the radiation detection threshold, i.e. the minimum level of prompt gamma radiation to which the device will respond. Note: it is recommended that the threshold resistor should remain within the range 500ohms to 60kohms.

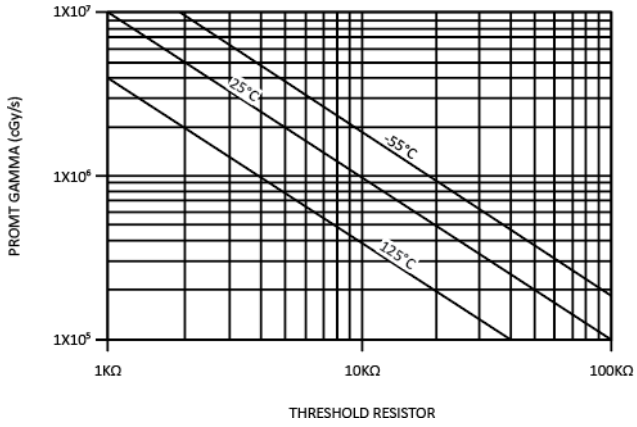

Figure 4. Radiation Detection Threshold vs Threshold Resistor Value (Vd = 5V)

As indicated in the previous graph, the radiation threshold varies with temperature i.e. decreases with increasing temperature. Figure 5 shows the extent of the variation. The vertical axis represents the normalized variation with respect to the radiation threshold at 25° C. Thus, a reading of 2 corresponds to twice the threshold at 25 °C.

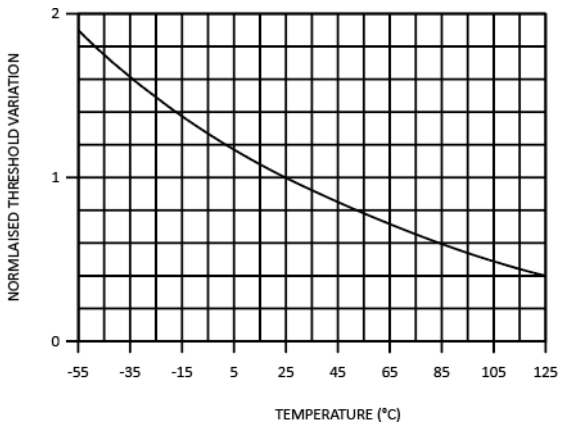

Figure 5. Gamma Dose Rate Threshold vs Temperature

10.0 Lockout Time

The lockout time is dependent on the value of the external programming capacitor. Figure 6 shows the relationship between the capacitor value and lockout time constant.

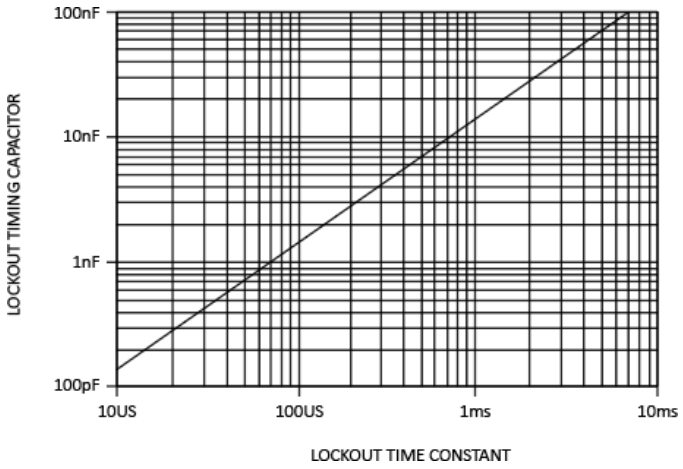

Figure 6. Lockout Capacitor Value vs Lockout Time Constant (25°)

Figure 7 shows how lockout time varies with dose rate. The vertical axis has been normalized with respect to the programmed lockout time constant at 25 °C. Thus, a value of 2 represents a lockout time of twice the time constant value at 25 °C. The horizontal axis is the product of gamma dose rate and threshold resistor value. Consider the following example.

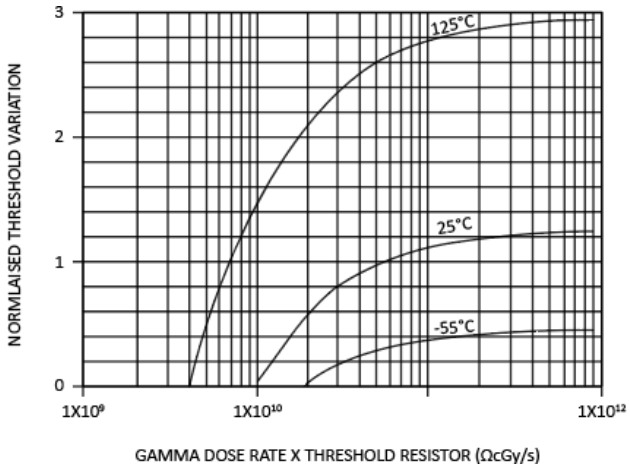

Figure 7. Variation of Lockout Time with Gamma Dose Rate / Threshold Resistor Product

Suppose the lockout time constant is 2 milliseconds and the threshold resistor is 10 kohms. If the gamma dose rate is 1E6 cGy/s, then the lockout time at 25° C is given by the point on the 25° C line corresponding the value 1E10, i.e. the point (1E10, 0).

At this level, the device would just trigger but the lockout time would be almost zero. If the dose rate were 2E6 the lockout time would be given by the point (2El0,0.6), i.e. 1.2 milliseconds (0.6 x 2ms).

As indicated by Figure 7, lockout time will also vary with temperature, i.e. increase with increasing temperature. Figure 8 shows the extent of this variation. Again, the vertical axis has been normalized with respect to the programmed lockout time constant at 25 °C.

For (Gamma Dose Rate * Threshold Resistor) > 4 x 10^{11} Ω Gy/s:

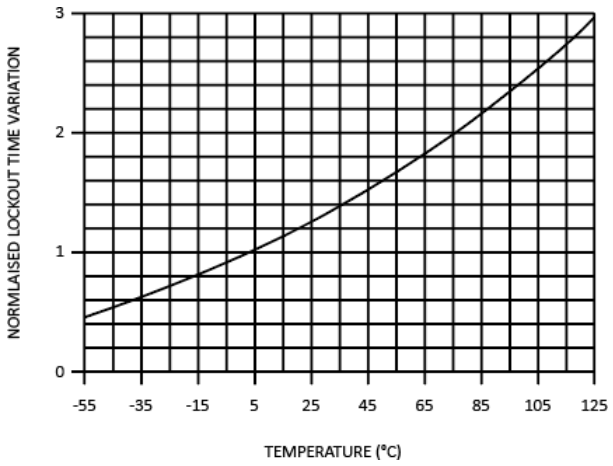

Figure 8. Variation of Lockout Time with Temperature

11.0 Built-in-Test

All of the circuitry within the NED can be exercised by activating the BIT input (0V at 100 mA) for > 50 µs. This induces a photo current in the PIN Diode event sensor, simulating the effect of a Nuclear Event and causing the device to trigger. Since the BIT induced photo current is fixed, BIT operation can be affected by the setting of the threshold setting resistor.

With the threshold resistor value below 15 kohms, the photo current generated by the internal BIT function may be insufficient to trigger the device. The circuit configuration shown below should therefore be used. Above 15 kohms, Rb and Cb may be omitted and the circuit may be reduced to the single component Rth.

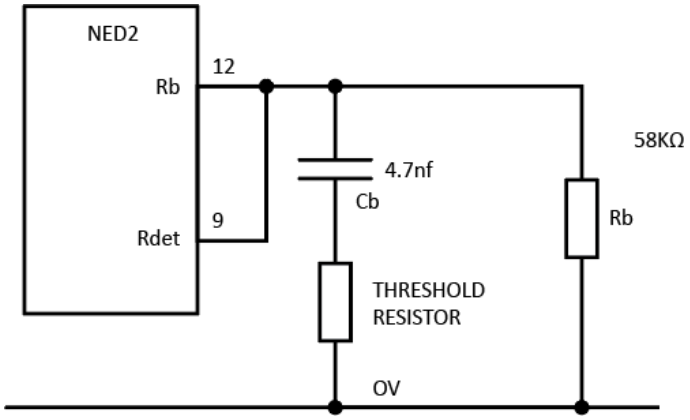

Figure 9. Circuit Configuration for Rth < 15Kohms

Note: the effective threshold resistance will be:

$$\frac{Rth \quad Rb}{Rth + Rb}$$

When Cb is charging

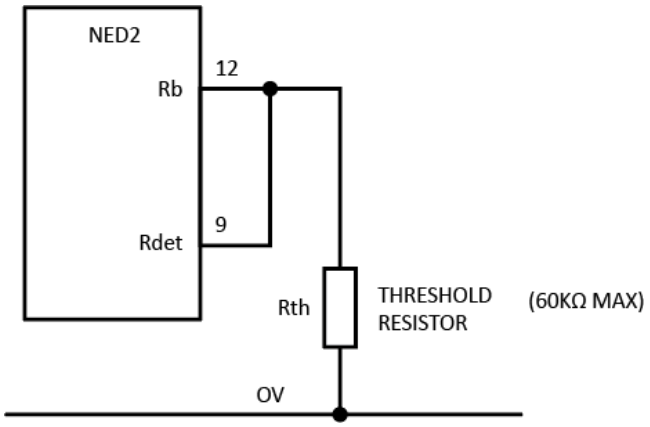

Figure 10. Circuit Configuration for Rth > 15Kohms

12.0 Vcc Connection

Correct operation of the NED requires a minimum of 4.5V power supply connected at all times, including during an event. Recommended values for C1 are:

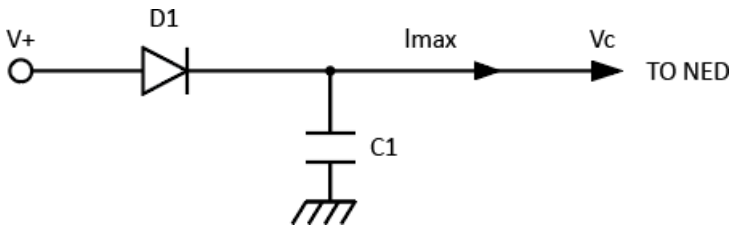

Figure 11. Vcc Connection

Assuming Vc = 5.0v Imax (operational) = 95mA minimum, capacitance = 190nF/µs of lockout time required. e.g. for 1ms lockout time, minimum capacitance value = 190µF.

Vc will be approx. 0.7V below V +, therefore V + should be 5.7V nominal.

13.0 WRITE Inhibit to Hard Memory

Even if a memory is radiation hardened, any data generated during an event may be corrupt and should not be stored.

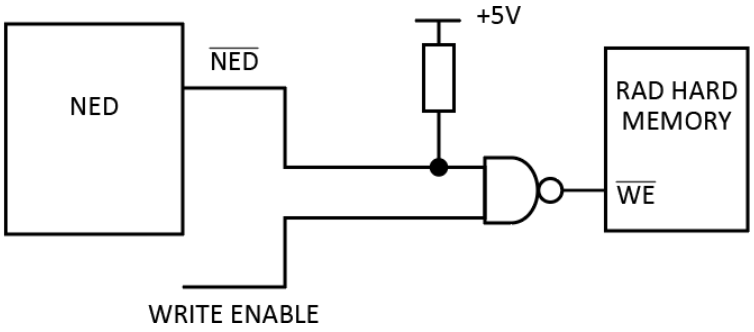

Figure 12. WRITE Inhibit to Hard Memory

14.0 Processor Protection During an Event

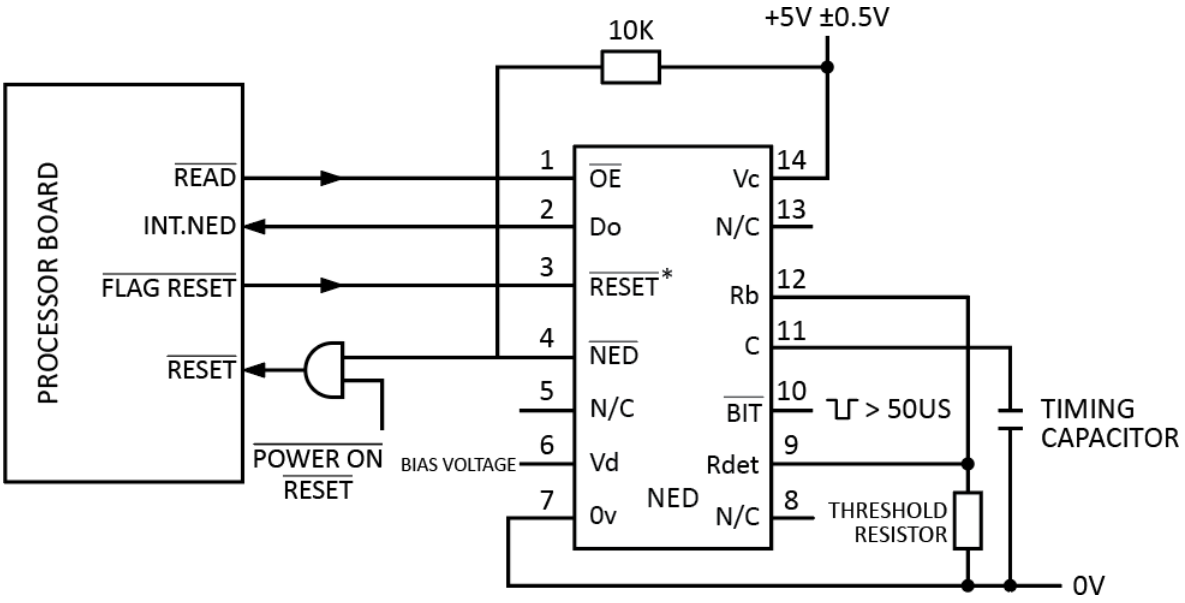

Figure 13. Processor Protection Diagram

**Note:*

1. *A Rising Edge on the RESET Input clears the Event Latch*
2. *The RESET Input is Inhibited internally whilst the NED Output is active*

15.0 Timing

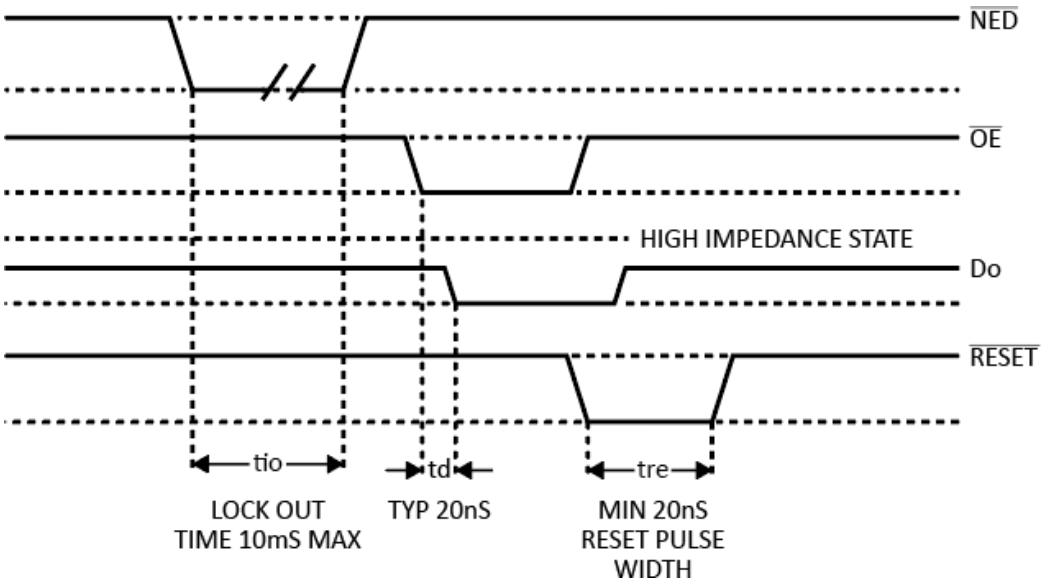

Figure 14. Timing Diagram

16.0 Ordering Information

MP1366/002